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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,557	04/09/2004	Anders Landin	5681-02301	1270

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EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 09/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,557	LANDIN ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-30 and 32-40* is/are rejected.

7)☒ Claim(s) *9 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the application filed 4/9/2004. Claims 1 are presented for examination and are currently pending.

In the response to this Office action, the Examiner politely requests that support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line numbers in the specification and/or drawing figure(s). This will assist the Examiner in prosecuting this application.

Excerpts from all prior art references cited in this Office action shall use the shorthand notation of [column # / lines A-B] to denote the location of a specific citation. For example, a citation present on column 2, lines 1-6, of a reference shall herein be denoted as "[2/1-6]."

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 13,15,16,22,37, and 38, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 13 it is not clear whether the --report--, the --address packet-- or both are generated by the memory. Nonetheless, for the purposes of examination, the Examiner has considered the limitation to mean the memory generates a report corresponding to the address packet, that was issued to the address network by the active device of claim 1. The Examiner suggests placing commas after --report-- and after --address packet-- to clarify the claim language.

As per claims 15, 16, 22, 37, and 38, it is not readily clear what the Applicant is trying to claim with regards to the active device being part of a single-node system, as base claim 1 clearly defines the active device being included in a system comprising both a --node-- **and** an --additional node--; therefore, the meets and bounds of the claims are not readily apparent. The active device as claimed in claim 1 is clearly included in a system with multiple nodes (i.e. the additional node), so the limitations defining a --single-node-- system are not coherent and therefore do not particularly point out and distinctly claim the subject matter which Applicant regards as the invention. No reasonable interpretation can be made by the Examiner and therefore, no art shall be applied against claims 15, 16, 22, 37, and 38, in this Office action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8,10-14,17-21,23-30,32-36,39, and 40, are rejected under 35 U.S.C. 102(b) as being anticipated by Singhal et al. (U.S. Patent No. 5,978,874).

As per claims 1 and 23, Singhal teaches:

(1) a node 510-1 (figure 1) including a memory 150-N (figure 2), and active device 160-N, an interface (combination of address controller 180 and bit-sliced data buffer 140) to an inter-node network (figure 1), and an address network (point-to-point connections between address controller 180 and devices 150-N, 160-N, and 170-N - [6/30-34]) coupling the memory, the active device and the interface (as shown in figure 2);

(2) an additional node 50-2 coupled to the node 50-1 by the inter-node network 20.

(3) wherein the active device is configured to initiate a transaction ([5/37-38] and [12/39-47]) to gain an access right (become a "writer") to a coherency unit (e.g. cache line or memory address) by sending and address packet on the address network (in order for the address controller 180 can send a request via the address bus 60) - [11/56/65];

(4) wherein if the transaction cannot be satisfied within the node 50-1 [7/5-8], the interface 180 is configured to send a coherency message to the additional node 50-2 (or whichever node owns the coherency unit) via the inter-node network 20 - [14/28-52]; and

(5) wherein in response to receiving an addition coherency message from the addition node via the inter-node network 20 [14/40-42], the interface 180 is configured to send data corresponding to the coherency unit to the active device 160-N [14/59-60]/[30/30-32], wherein the active device gains the access right (ability to write the data) upon receipt of the data [28/3-5] and [28/23-25] - the device cannot become a "writer" to the cache line data until the data packet has been received.

As per claims 2 and 24, the address packet may be a read-to-own packet [14/18-27] and the access right is a write access right [14/23-25].

As per claims 3 and 25, an additional interface (e.g. the address controller 180 and the data buffer 140 of the additional node 50-2) included in the additional node is configured to receive the coherency message (foreign read-to-own message) [7/5-7] and to responsively send a proxy-read-to-own modified packet (e.g. the instructions sent by the receiving node's interface 180 to invalidate its copies of the cache line [14/56-57] by means of invalidating all of its CPUs that may have a copy of the cache line - [14/61-63]) on an additional address network (that links the CPUs 160 and 170 and the memory 150 [6/30-34] of the additional node) included in the additional node.

As per claim 4 and 26, an additional active device (processors 160-170) included in the additional node 50-2 is configured to lose an ownership responsibility for the coherency unit upon receipt of the proxy-read-to-own modified packet - [14/57-60].

As per claims 5 and 27, wherein the additional active device 160 in the additional node 50-2 is configured to send a data packet corresponding to the coherency unit on an additional data network (connection between additional node's data buffer 140 and the inter-node's data

bus 70) included in the additional node (figure 2) in response to receiving the proxy read-to-own modified packet [14/59-60], wherein the additional active device transitions an access right to the coherency unit upon sending the data packet (e.g. transitions to invalid - [14/57-59]).

As per claims 6 and 28, wherein the additional active device in the additional node is configured to send the additional coherency message on the inter-node network 20 (as the data bus 70 connects between the nodes - figure 2) response to receiving the data packet sent by the additional active device (relinquishes modified data - [14/59-60]), wherein the additional coherency message includes a copy of the coherency unit - [14/64-66].

As per claims 7 and 29, Singhal teaches:

(1) wherein in response to receiving the coherency message, the additional interface (180 of node 50-2) is configured to send a proxy-read-to-own packet (packet used to invalidate the processors of the additional node which own the copy of the cache line - [14/56-59] on an additional address network (connection between address controller 180 to the memory and CPUs) included in the additional node 50-2;

(2) wherein in response to receiving the proxy-read-to-own packet, a plurality of additional active devices (160-170) included in the additional node 50-2 are configured to invalidate an access right (i.e. if they have cache a copy) to the coherency unit - [14/56-63] and [29/4-6]; and

(3) wherein the additional interface 180 is further configured to send an invalidating coherency message (i.e. it may send its own read-to-own request for a coherency unit to request a certain cache line requested by its own processor 160 or 170 - [14/19-27] - in this case, since the read-to-own message results in invalidations [28/32-34], the Examiner is considering the read-to-

own transaction to be an invalidating coherency message) on the inter-node network to one or more other nodes [28/32-34] that include active devices (160,170) having a read access right (i.e. shared) to the coherency unit (the additional interface broadcasts the read-to-own request to all other nodes [14/31-34] and [28/32-34], thereby, all other nodes that include active devices having a read access right are invalidated).

As per claims 8 and 30, in response to the invalidating coherency message (in this case the read-to-own message and described above), interfaces included in each of the one or more other nodes are configured to send a proxy-invalidate coherency message (i.e. a necessarily inherent message such that all copies of the coherency unit within the respective caches of the CPUs 160-170 are invalidated - [28/32-34]) on a respective address network (connection between address controller 180 and the respective CPUs 170-180) and to send an acknowledge coherency message [29/4-6] to the node 50-1 in response to receiving the proxy-invalidate coherency message on the respective address network. It is noted that while the system of Singhal does not specifically wait for invalidation acknowledgements to arrive, Singhal teaches that such acknowledgements are required [28/66-29/3].

As per claims 10 and 32, an additional memory 160 included in the additional node 50-2 (in this case the home node) is configured to send data corresponding to the coherency unit to the additional interface 180 (as shown in figure 2) [14/42-47] in response to receiving the proxy read-to-own packet (i.e. the message sent to the memory 160 of the home node via the point-to-point connection from the address controller 180 in order to fetch the requested data); and wherein the additional interface 180 is configured to include the data in the additional coherency message sent to the [requesting] interface included in the node - [14/40-52].

As per claims 11 and 33, wherein the additional node is a home node for the coherency unit - [14/40-52] and [13/50-52].

As per claims 12 and 34, wherein the interface 180 is configured to send the coherency message in response to an indication that the transaction cannot be completed within the node (e.g. the requesting node is not the owner or the home node of the request coherency unit - [14/18-27]), wherein the indication is an address (i.e. a requested address of a cache miss), wherein the address of the coherency unit does not mapped (i.e. is not contained or the home node for the requested coherency unit) to any memory included in the node. Since the requesting node is not the home node for the cache line, a request must be sent on the inter-node network 20 to determine the owner/home node to retrieve the data [13/50-52] and [30/27-30].

As per claims 13 and 35, the Examiner is considering the Dtag RAM 220 portion of the node to be part of the node's memory, which comprises the DTAG 220 and memory 150. DTAG 220 comprises the global access states (shared, owned, invalid, modifier) of coherency units cached throughout the system - [23/17-20]. If a device within the node caches a copy of a SHARED coherency unit, but another unit outside the node is the owner, the transaction to acquire ownership cannot be completed within the node [14/35-39] since the Address of the coherency unit must be sent on the Address Bus 60 in order to inform the owner of the coherency unit to invalidate the line [14/54-60]. It could therefore be seen that the DTAG 220 portion of the --memory--, maintaining the state list of the coherency units, would be used to filter the corresponding global access state of the Shared coherency unit using the tag address of the requested coherency unit [6/64 - 7/16] and indicate a report (i.e. the return of the indication that the coherency unit is SHARED with another device in another node). It follows that based on

the report from the DTAG portion of the memory that the interface 180 is required to send the coherency message (read-to-own) onto the inter-node network 20 so that the other device caching a copy of the coherency unit can be invalidated and ownership can be exchanged.

As per claims 14 and 36, the active device does not implement different operating modes based on whether a given coherency unit maps or does not map to a memory within the node. Singhal does not mention a node 50-1 operating in different modes, and instead teaches one method to perform cache coherency throughout the network 10. If the coherency unit maps to the memory within the node (i.e. the cache line can be found in the unit) the operating mode of the coherency scheme may determine that the another node may have a shared copy of the data and a local device wishes to have exclusive access (where a read-to-own packet needs to be sent) - [14/35-39]. If however, the coherency unit does not map to the memory within the node (i.e. the cache line is contained in another node), the same operating procedure is used where the address controller 180 drives the address bus in order to send a read-to-own packet to the other nodes in the system; however, in this case, since the data was not mapped to the requesting node, the data is returned from the owner - [14/59-60].

As per claims 17 and 39, the active device is configured to send a same type of address packet containing a same type of command encoding (command encoding for a read-to-own packet) to initiate the transaction for the coherency unit if the coherency unit does not map (e.g. a valid copy is not contained in the node) [14/21-34] to any memory in the node as the active device is configured to send to initiate the transaction for the coherency unit if the coherency unit does map (e.g. the device contains a valid copy of data but requests ownership in which to write the cache line) to the memory included in the node [14/35-37].

As per claims 18 and 40, similar to claim 17, the active device uses the same type of address packet (i.e. address requested as part of a read-to-own transaction packet) regardless of whether the transaction can be satisfied within the node - [14/61-63]. Even though the invalidation of the read-to-own packet could have been satisfied by only invalidating the shared copies within the same node as the requestor - [14/61-63], the active device sends the read-to-own request on to the address controller 180 of the interface to broadcast the read-to-own packet to make sure other devices caching the requested line are invalidated as well [14/53-60].

As per claims 19 and 20, lines 1-7 were discussed with respect to claim 1. To gain access to a coherency unit, the active device sends an address packet including a command encoding (read-to-own) on the address network (connection between interface 180 and CPUs/memory 150-170) wherein the coherency unit maps to the memory subsystem (the requesting device already contains the data but in a shared state and would like to write to the coherency unit - [14/35-39]). Further, as discussed in the rejection of claims 14 and 17, supra, if the coherency unit does not map to the memory subsystem (i.e. collection of all memory of the node including memory 150 and inherent - but not shown - caches of the active devices 160 and 170) whereas the active requesting device does not contain a copy of the requested cache line, a read-to-own encoding is still used and the interface 180 is used to send a coherency message corresponding to the additional address packet to the additional node 50-2 via the inter-node network 20 in response to receiving the additional packet [14/62-63].

As per claim 21, the encoding may be a read-to-share, where the right access is a read access - [13/30 - 14/12].

Allowable Subject Matter

Claims 9 and 31 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

As per claims 9 and 31, Singhal teaches away from withholding data until an acknowledgement coherency message has been received from each of the one or more other nodes as taught in [28/63 -29/14].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hum et al. (U.S. Patent Application Publication No. 2004/0123047) teaches a node system comprising an import and export cache.

Sharma et al. (U.S. Patent No. 6,108,737) teaches using a commit-signal in a node cluster system for expediting operation completion.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas

PIERRE BATAILLE
PRIMARY EXAMINER
9/25/06